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Insulated gate type semiconductor device

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SPECIFICATION

1. TITLE OF INVENTION

Insulated gate type semiconductor device

2. CLAIMS

1. An insulated gate type semiconductor device wherein a channel formation region of an insulated gate type field effect transistor comprises a non-single crystal semiconductor added with hydrogen or halogen elements, a pair of impurity regions constituting a source and a drain neighboring said semiconductor has crystal growth promoted more than that of said non-single crystal semiconductor, and said regions having crystal growth promoted are provided as to extend to said channel formation region under the gate electrode.

2. The insulated gate type semiconductor device of Claim 1 wherein the channel formation region added with hydrogen or halogen elements at a concentration of 1 atom% or more comprises a non-single crystal semiconductor and a semiconductor with crystal growth promoted more than that of said non-single crystal semiconductor.

3. DETAILED DESCRIPTION OF THE PRESENT INVENTION

"Field for Industrial Use"

The present invention relates to an insulated gate type field effect semiconductor device (hereinafter referred to as IGF) utilized for a semiconductor integrated circuit, a liquid crystal display panel, etc.

"Prior Art"

IGFs utilizing single crystal silicon are widely utilized in the field of semiconductors. A typical example is Japanese Patent Pub.

No. Sho 50-1986 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor. However, with regard to IGF whose channel formation region not added with hydrogen is not made of a single crystal semiconductor, but made of a non-single crystal semiconductor added with hydrogen or halogen elements at a concentration of 1 atom% or more, a typical example is shown in Japanese Pat. Appl. No. Sho 53-124021 "SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" invented by the present inventor (filed on October 7, 1978).

This IGF whose channel formation region comprises a semiconductor, especially a silicon semiconductor added with hydrogen or halogen elements, has OFF-state current of $1/10^3$ to $1/10^5$ of that of the conventional IGF utilizing a single crystal semiconductor. Therefore it is believed that this IGF is used effectively for controlling a liquid crystal display panel. As in the example above mentioned, there are three types of semiconductors as this IGF: there are a lateral channel type IGF wherein a gate electrode is formed on a semiconductor of a channel formation region, a vertical channel type IGF mentioned in Japanese Pat. Appl. No. Sho 56-001767 "INSULATED GATE TYPE SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD THEREOF" by the present inventor (January 9, 1981), and a conventional thin film IGF transistor type wherein a gate electrode is provided beneath a semiconductor composing a channel formation region. Compared with the latter two, the structure of the former is the same as that of the conventionally known IGF utilizing single crystal silicon. Thus this IGF has a superiority that established technologies can be applied.

However, a source and a drain of this IGF should be formed not through a CVD method (including a plasma CVD method) by deposition of a thin film, but through ion implantation, etc. Donors and acceptors have to be activated by annealing under a temperature of 400 °C or less, which is the range hydrogen or halogen elements are

not deaired. In addition, improvement in reverse breakdown voltage between the source and the drain, especially between the drain and the channel formation region, is demanded.

"Means to Solve the Problems"

The present invention aims to solve the problems above mentioned. A gate insulator and a gate electrode above it are selectively formed on a non-single crystal semiconductor with no or little doped impurities (hereinafter non-single crystal semiconductor added with hydrogen or halogen elements is simply referred to as a semiconductor, or a non-single crystal semiconductor). Utilizing this gate electrode as a mask, impurities for the source and the drain are added by an ion implantation method or the like. For example, phosphorous or arsenic is added for N channel type, and boron is added for P channel type, into the non-single crystal semiconductor to constitute impurity regions. After that, strong light is irradiated at 400 °C or less to the regions added with these inactive impurities, thereby performing strong light anneal (hereinafter simply referred to as light anneal). Thus the semiconductor is transformed into a semiconductor with hydrogen or halogen elements added and retained, and with crystallinity promoted more than that of the channel formation region, particularly a semiconductor with a polycrystal or single crystal structure. Moreover, by extending this crystallization to the channel formation region, PI or NI junctions are made into regions with high crystallinity. In this manner, to improve breakdown voltage between the junctions and a non-single crystal semiconductor added with hydrogen or halogen elements for reducing OFF-state current, polycrystal regions or single crystal regions are provided in the channel formation region near the PI or NI junction interfaces.

"Results"

As a result, in the structure of the IGF of the present invention, junction breakdown voltage of a source and a drain, especially of a drain, can be made as high as that of a single crystal semiconductor. Compared with a thin film transistor including the conventional amorphous semiconductor, the breakdown voltage is higher by nearly 20 V. In addition, a gate electrode is provided above a non-single crystal semiconductor composing a channel formation region on a substrate. Active impurity regions having optical Egs of 1.6 to 1.8 eV which is approximately the same as that of optical Eg (1.7 to 1.8 eV in the case of a silicon semiconductor) of this non-single crystal semiconductor are obtained. Since Eg is the same as or approximately the same as that of the channel formation region, ON-state current flows smoothly at rise time, and OFF-state current will not llikely to flow sluggishly at fall time. In other words, OFF-state current is less and ON/OFF can be switched with high speed response.

The present invention is explained according to the following embodiment.

"Embodiment 1"

As shown in Fig.1 (A), a quartz glass substrate of 10 cm x 10 cm large and 1.1 mm thick is utilized as a substrate (1). A non-single crystal semiconductor (2) including an amorphous structure added with hydrogen at a concentration of 1 atom% or more is formed in a thickness of 0.2μ by a plasma CVD (high frequency of 13.56 MHz, substrate temperature of 210 °C) of silane (SiH_4). A silicon nitride film (3) is deposited thereon as a gate insulating film by a photo CVD method. That is, Si_3N_4 is formed in a thickness of 1000 Å by a reaction of Si_2H_6 with ammonia or hydrazine (a low pressure mercury lamp including a wavelength of 2537 Å and a substrate temperature of

250 °C) without utilizing mercury enhancing method.

Then portions other than a region (5) composing an IGF are removed by a plasma etching method. This reaction is performed as $CF_4 + O_2$ (5%) at 13.56 MHz at a room temperature. A microcrystal or polycrystal semiconductor of N^+ conductivity type is deposited in a thickness of 0.3 μ on this gate insulating film. This N^+ semiconductor film is removed utilizing a resist (6) by a photoetching method. Then phosphorous is added to the regions to be a source and a drain utilizing this resist and an N^+ semiconductor gate electrode portion (4) as a mask by an ion implanting method at a concentration of 1×10^{20} cm^{-3}, as shown in Fig.1 (B). Thus a pair of impurity regions (7) and (8) are formed.

After the resist of the gate electrode is removed, strong light (10) anneal is performed on the whole substrate. That is, light is irradiated in a linear shape utilizing an extra-high pressure mercury lamp (output of 5 KW, wavelength of 250 to 600 nm, diameter of 15 mmϕ, length of 180 mm) having a parabolic reflection mirror at its back side and a quartz cylindrical lens (focal distance of 150 cm, converging width of 2 mm, length of 180 mm) in its front. The irradiated part of the substrate is scanned at a speed of 5 to 50 cm/min. to have strong light irradiate to the entire surface of the substrate of 10 cm x 10 cm. Because a large amount of phosphorous has been added to the gate electrode portion, this electrode absorbs enough light and polycrystallizes itself. The impurity regions (7) and (8) once dissolve and recrystallize. They dissolve in the direction of scanning, that is, in the direction of X. Recrystallization is shifted (transported). As a result, compared with the case of merely heating or irradiating the entire substrate evenly, grain size of crystals can be made bigger because a system of crystal grain growth has been added.

This region which has been polycrystallized reaches the entire

peripheral region of the impurity regions. As shown in the figure, the bottom of this polycrystallized region reaches even the substrate (1). As shown by broken lines (11) and (11'), the polycrystallized regions extend into the channel formation region beyond junction interfaces (17) and (17') of the impurity regions (7) and (8) by 0.3 to 3 μ. Morphological interfaces (15) and (15') are provided under the gate electrode. That is, the ends (15) and (15') extend into the channel formation region beyond the ends of the gate electrode (16) and (16'). Because N (7), (8) - I (2) junction interfaces (17) and (17') are provided inside of the crystallized region, high breakdown voltage against the reverse bias is gained so that high breakdown voltage IGF can be formed. The crystallized semiconductor region in the I type semiconductor can be determined by scanning speed and intensity (the level of irradiation) of light anneal.

In the figure, after the process in Fig.1 (B), PIQ is coated on the whole surface in a thickness of 2 μ, and formed as electrode holes (13) and (13'), then as ohmic contact of aluminum and its leads (14) and (14'). In the process of forming these (14) and (14') being a second layer, they can be connected with the gate electrode (4).

As a result of this light anneal, sheet resistance of the impurity regions changed from 4×10^{-3} $(\Omega cm)^{-1}$ before light irradiation to $1 \times 10^{+2}$ $(\Omega cm)^{-1}$. This change in the electric conductivity characteristic is clearly shown.

As shown in curved line (21) of Fig.2, drain breakdown voltage can be made up to 60 V in the case that the length of the channel formation region is 10 μ and the width of the channel is 1 mm. This is a condition when the gate voltage is at V_{GG} = 10 V. This drain breakdown voltage is a great improvement compared with the conventionally known thin film transistor wherein junction region of

an amorphous structure has drain breakdown voltage widely varying from 30 to 50 V.

"Effects"

Because the present invention utilizes the manufacturing process of forming and processing films gradually from lower levels, large-area large-scale integration is realized. Therefore as many as 500 x 500 pieces of IGFs can be formed in a 30 cm x 30 cm panel, and can be utilized as IGFs for controlling liquid crystal display elements.

A semiconductor which has been polycrystallized or single crystallized by light anneal process is extended to the channel formation region. As a result, the drain breakdown voltage is increased more than that of the conventional method, by 20 V or more.

As this light anneal utilizes ultraviolet rays, crystallization from the surface of the semiconductor to the portion inside is promoted. Thus electric current flowing through the channel formation region near the gate insulating film to the fully polycrystallized or single crystallized impurity regions near the surface can be controlled with no problem.

Single crystal semiconductors are not at all utilized as substrates. Thus the portion inside of the channel formation region apart from the source and the drain can keep the state as a non-single crystal semiconductor without being influenced by the light irradiation anneal process. Therefore OFF-state current can be made $1/10^3$ to $1/10^4$ of that of a single crystal semiconductor.

Because the source and the drain are formed by light anneal after formation of the gate, the interface with the gate insulator will not be contaminated and its characteristic is stable. Unlike the conventional method, not only quartz glass but also soda glass, and a heat endurable organic film can be utilized as optional substrate materials.

The formation of a semiconductor - a gate insulator - a gate electrode comprising a channel formation region of interfaces of different materials and the processes in the same reaction chamber can be performed without being exposed to the air. Thus it is characterized in that interface traps are rarely generated.

In the present invention, it is preferable that each impurity concentration of oxygen, carbon and nitrogen in the non-single crystal semiconductor of the channel formation region is 5×10^{18} cm^{-3} or less. In the conventionally known IGF, impurities are mixed in the channel layer at a concentration of 1 to 3×10^{20} cm^{-3}. In the case of utilizing an amorphous silicon semiconductor, life time of carriers, especially that of holes, are shortened. Thus in terms of characteristics, current flown is as little as 1/3 or less of that of the present invention. In addition, hysteresis characteristic is observed when drain electric field is applied at 2×10^6 V/cm or more to I_{DD} - V_{GG} characteristic. On the other hand, when oxygen is 5×10^{18} cm^{-3} or less, hysteresis is not observed even with an electric potential of 3×10^6 V/cm.

4. BRIEF DESCRIPTION OF THE FIGURES

Fig.1 shows cross sectional views of the manufacturing process of the insulated gate field effect semiconductor device of the present invention.

Fig.2 shows characteristic of drain current - drain voltage.

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